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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/897,902	07/05/2001	Isamu Hayashi	XA-9512	1411

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
LEE, CHRISTOPHER E	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 10/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/897,902	HAYASHI ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 26th of July 2004. Claims 1-14 have been amended; no claim has been canceled; and no claim has been newly added since the Non-Final Office Action was mailed on 26th of January 2004. Currently, claims 1-14 are pending in this application.

Claim Objections

2. Claim 14 is objected to because of the following informalities:

Substitute "A microprocessor" in line, by --The microprocessor--.

Claim Rejections - 35 USC § 102

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Kume et al. [JP 405341872 A; cited by the Applicants; hereinafter Kume].

Referring to claim 2, Kume discloses a microprocessor (i.e., microprocessor 1 of Fig. 1) comprising: a central processing unit (i.e., central processing unit 2 of Fig. 1) for executing instructions (See Fig. 1 and col. 5, para. [0022]; i.e., wherein in fact that the Fig. 1 shows the address bus 8 and the data bus 7 coupled to said central processing unit, and said central processing unit outputting access address inherently anticipates that said central processing unit executing instructions); an external bus interface control circuit (i.e., micro controller 15, control register 14 and clock selection logic 18 in Fig. 1) which controls an external bus (i.e., system data bus 9 and system address bus 10 in Fig. 1) based on execution of instructions by said central processing unit (i.e., based on external access operation by said central processing unit; See col. 4, para. [0021]), wherein said external bus interface control circuit is capable of activating either a first external device select signal or a second external device select signal corresponding to an external access address (See col. 5, para. [0029] and [0030]), wherein said

microprocessor includes a clock switching control circuit (i.e., clock output selection switch 20 of Fig. 1) and a clock pulse generator (i.e., clock generator 30 and counting-down circuit 19 in Fig. 1), wherein said clock switching control circuit (i.e., clock output selection switch) controls an operation to switch a synchronous clock signal of said external bus interface control circuit to a first clock signal in accordance with activation of said first external device select signal or to a second clock signal in accordance with activation of said second external device select signal (See col. 5, para. [0024]), and wherein said clock pulse generator generates said first clock signal (i.e., clock signal for the first external data processing device 22 in Fig. 2) and said second clock signal (i.e., clock signal for the second external data processing device 23 in Fig. 2), and said first clock signal is a predetermined frequency different from that of second clock signal (i.e., said counting-down circuit generates different frequencies on the parallel signal lines).

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kume [JP 405341872 A] in view of Kakiage [US 5,916,311 A].

Referring to claim 1, Kume discloses a microprocessor (i.e., microprocessor 1 of Fig. 1) comprising: a central processing unit (i.e., central processing unit 2 of Fig. 1) for executing instructions (See Fig. 1 and col. 5, para. [0022]; i.e., wherein in fact that the Fig. 1 shows the address bus 8 and the data bus 7 coupled to said central processing unit, and said central processing unit outputting access address inherently anticipates that said central processing unit executing instructions); an external bus interface control circuit (i.e., micro controller 15, control register 14 and clock selection logic 18 in Fig. 1), coupled to said central processing unit (i.e., said micro controller, control register and clock selection logic are coupled to said central processing unit via internal address bus 8 in Fig. 1), which controls an external bus (i.e., system data bus 9 and system address bus 10 in Fig. 1) based on execution of

instructions by said central processing unit (i.e., based on external access operation by said central processing unit; See col. 4, para. [0021]), said external bus interface control circuit being capable of selecting one of a plurality of external device select signals corresponding to an external access address and activating said selected external device select signal (See col. 5, para. [0029] and [0030]); a clock generation circuit (i.e., clock generator 30 and counting-down circuit 19 in Fig. 1), coupled to said central processing unit and said external bus interface control circuit (i.e., said clock generator and counting-down circuit are coupled to said central processing unit, said micro controller, control register and clock selection logic via internal signal connection in Fig. 1), to generate a plurality of clock signals (See col. 5, para. [0023]); a clock switching control circuit (i.e., clock output selection switch 20 of Fig. 1), for controlling an operation to switch said plurality of clock signals in accordance with said external device select signal activated by said external bus interface control circuit (See col. 5, para. [0024]); a first clock terminal (i.e., a first terminal from said counting-down circuit 19 in Fig. 1), coupled to said clock generating circuit (i.e., clock generator and counting-down circuit), to supply a first clock signal to a first external device (i.e., a first clock signal for the first external data processing device 22 in Fig. 2); and a second clock terminal (i.e., a second terminal from said counting-down circuit 19 in Fig. 1), coupled to said clock generating circuit (i.e., clock generator and counting-down circuit), to supply a second clock signal to a second external device (i.e., a second clock signal for the second external data processing device 23 in Fig. 2), in parallel with said first clock signal (i.e., said second clock signal from said counting-down circuit being in parallel with said first clock signal from said counting-down circuit), said second clock signal having a different frequency from said first clock signal (i.e., said counting-down circuit generates different frequencies on the parallel signal lines).

Kume does not expressly teach a synchronous clock signal is provided to said external bus interface control circuit in accordance with said external device select signal activated by said external bus interface control circuit.

Kakiage discloses a bus controller (See Abstract and Fig. 1), wherein a synchronous clock signal (i.e., synchronous clock selecting signal 110 of Fig. 1) is provided to an external bus interface control circuit (i.e., external access controlling signal generator 8 of Fig. 1) in accordance with an external device select signal (i.e., space identifying signal 107 of Fig. 1) activated by said external bus interface control circuit (See col. 9, lines 31-35; i.e., wherein in fact that the external access controlling signal generator generates a bus cycle signal for indicating an external bus cycle period and a data output signal for indicating a timing at which data is to be output to the external data bus at the time of writing to the external device inherently implies that said external device select signal (i.e., space identifying signal) is activated by said external bus interface control circuit (i.e., external access controlling signal generator)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said bus controller, as disclosed by Kakiage, in said microprocessor, as disclosed by Kume, for the advantage of providing a bus controller, wherein an external bus cycle time optimal for the access time to said external device can be obtained (See Kakiage, col. 6, lines 46-49).

However, the recitation in the preamble, such that "a microprocessor built on a semiconductor chip", has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *See Kropa v. Robie, 88 USPQ 478 (CCPA 1951).*

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kume [JP 405341872 A] as applied to claim 2 above, and further in view of Yanagiuchi [US 5,684,418 A].

Referring to claim 3, Kume discloses all the limitations of the claim 3 including clock output pin (i.e., pin for clock signal line 21 in Fig. 1), and wherein said clock output pin supplies said first and second clock signals generated by said clock pulse generator in parallel (i.e., said clock pulses are generated from counting-down circuit in parallel; See col. 5, para. [0024]), except that does not teach

clock output pins supply respectively said first and second clock signals generated by said clock pulse generator.

Yanagiuchi discloses a clock signal generating system (Fig. 1), wherein clock output pins (i.e., clock signal output lines from clock generator 1 in Fig. 1) supply respectively a first clock signal (e.g., clock output from X_2 11-2 in Fig. 1) and a second clock signal (i.e., clock output from $X_{1/2}$ 12-2 in Fig. 1) generated by a clock pulse generator (i.e., clock generator 1 of Fig. 1; See col. 3, lines 26-47). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said clock generator and said clock selector in said clock signal generating system, as disclosed by Yanagiuchi, for said clock pulse generator and said clock switching control circuit, respectively, as disclosed by Kume, for the advantage of providing a clock signal generator which can make a multiplier and a frequency divider generating a frequency which is not being used stop and thereby prevent needless power consumption and achieve a low power consumption of a system or chip as whole (See Yanagiuchi, col. 1, lines 44-49).

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kume [JP 405341872 A] in view of Blomgren et al. [US 5,381,543 A; hereinafter Blomgren].

Referring to claim 4, Kume discloses a microprocessor comprising: Kume discloses a microprocessor (i.e., microprocessor 1 of Fig. 1) comprising: a central processing unit (i.e., central processing unit 2 of Fig. 1) for executing instructions (See Fig. 1 and col. 5, para. [0022]; i.e., wherein in fact that the Fig. 1 shows the address bus 8 and the data bus 7 coupled to said central processing unit, and said central processing unit outputting access address inherently anticipates that said central processing unit executing instructions); an external bus interface control circuit (i.e., micro controller 15, control register 14 and clock selection logic 18 in Fig. 1) controlling an external bus (i.e., system data bus 9 and system address bus 10 in Fig. 1) based on execution of instructions by said central processing unit (i.e., a basis of external access operation by said central processing unit; See col. 4, para. [0021]), wherein said

external bus interface control circuit is capable of activating either a first external device select signal or a second external device select signal corresponding to an external access address (See col. 5, para. [0029] and [0030]), and a clock switching control circuit (i.e., clock output selection switch 20 of Fig. 1), capable of: switching a synchronous clock signal of said external bus interface control circuit to a first clock signal (e.g., clock signal 21 for the external data processing device 22 in Fig. 2) and a synchronous clock signal of said central processing unit to said first clock signal (i.e., clock signal 52 for CPU 2 in Fig. 1, which is coincided with said clock signal 21 for the external data processing device 22 in Fig. 2) in response to activation of said first external device select signal, and switching said synchronous clock signal of said external bus interface control circuit to a second clock signal (e.g., clock signal 21 for the external data processing device 23 in Fig. 2) and said synchronous clock signal of said central processing unit to said second clock signal (i.e., clock signal 52 for CPU 2 in Fig. 1, which is coincided with said clock signal 21 for the external data processing device 23 in Fig. 2) in response to activation of said second external device select signal (See col. 5, para. [0024]), wherein a frequency of said first clock signal is different from a frequency of said second clock signal, and said first clock signal and said second clock signal are provided in parallel and external to said microprocessor (i.e., said counting-down circuit generates different frequencies on the parallel signal lines, and being provided to external devices in Fig. 1).

Kume does not teach said clock switching control circuit is capable of supplying a third clock signal to said central processing unit as well as supplying said first clock signal, and is capable of supplying a fourth clock signal to said central processing unit as well as supplying said second clock signal, wherein a frequency of said first clock signal is different from a frequency of said third clock signal, a frequency of said second clock signal is different from a frequency of said fourth clock signal.

Blomgren discloses a dual clock mechanism (i.e., clock 422, PLL 402 and write back cache 420C, Bus Converter 420D and their signal connections in Fig. 4), wherein said dual clock mechanism is capable of

supplying a third clock signal (e.g., 66MHz in Fig. 4) to a central processing unit (i.e., CPU 420A of Fig. 4) as well as supplying a first clock signal (i.e., 33MHz in Fig. 4), and is capable of supplying a fourth clock signal (e.g., other frequency 300MHz) to said central processing unit as well as supplying a second clock signal (i.e., 150MHz; See col. 7, lines 8-14), wherein a frequency of said first clock signal is different from a frequency of said third clock signal (i.e., two different frequencies 33MHz and 66MHz in Fig. 4), a frequency of said second clock signal is different from a frequency of said fourth clock signal (i.e., two different frequencies 150MHz and 300MHz).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said dual clock mechanism, as disclosed by Blomgren, in said microprocessor, as disclosed by Kume, for the advantage of providing a means for operating said central processing unit (i.e., CPU) in said microprocessor (i.e., single chip microprocessor) at a multiple of the cycle speed of a memory bus (See Blomgren, col. 2, lines 30-32).

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kume [JP 405341872 A] in view of Blomgren [US 5,381,543 A] as applied to claim 4 above, and further in view of Yanagiuchi [US 5,684,418 A].

Referring to claim 5, Kume, as modified by Blomgren, discloses all the limitations of the claim 5 including a clock pulse generator (i.e., clock generator 30 and counting down circuit 19 in Fig. 1; Kume) and clock output pin (i.e., pin for clock signal line 21 in Fig. 1; Kume), wherein said clock pulse generator generates said first clock signal, said second clock signal (i.e., generating clock signals whose frequencies are different; See Kume, col. 5, para. [0023]), said third clock signal, said fourth clock signal (See Blomgren, col. 7, lines 8-14), and wherein said clock output pin outputs said first and second clock signals generated by said clock pulse generator (See Kume, col. 5, para. [0024]), except that does not teach clock output pins supply respectively said first and second clock signals generated by said clock

pulse generator, and wherein each of said third and fourth clock signal frequencies is that of said first clock signals.

Yanagiuchi discloses a clock signal generating system (Fig. 1), wherein clock output pins (i.e., clock signal output lines from clock generator 1 in Fig. 1) supply respectively a first clock signal (e.g., clock output from X_2 11-2 in Fig. 1) and a second clock signal (i.e., clock output from $X_{1/2}$ 12-2 in Fig. 1) generated by a clock pulse generator (i.e., clock generator 1 of Fig. 1; See col. 3, lines 26-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said clock generator and said clock selector in said clock signal generating system, as disclosed by Yanagiuchi, for said clock pulse generator and said clock switching control circuit, respectively, as disclosed by Kume, as modified by Blomgren, for the advantage of providing a clock signal generator which can make a multiplier and a frequency divider generating a frequency which is not being used stop and thereby prevent needless power consumption and achieve a low power consumption of a system or chip as whole (See Yanagiuchi, col. 1, lines 44-49).

Thus, Kume, as modified by Blomgren and Yanagiuchi, impliedly suggests each of said third and fourth clock signal frequencies is that of said first clock signal (See Blomgren, col. 7, lines 8-14; i.e., wherein in fact that other frequencies could be used for said clock signals, and other multiples could be used for said multipliers implies that each of said third and fourth clock signal frequencies is that of said first clock signal).

10. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kume [JP 405341872 A] as applied to claim 2 above, and further in view of Fujita [US 6,529,083 B2].

Referring to claim 6, Kume discloses all the limitations of the claim 6 except that does not teach said clock switching control circuit requests said central processing unit to suspend execution of instructions in response to activation of a selected external device select signal, and wherein said clock switching control circuit is further capable of switching said first clock signal which is provided to said

external bus interface control circuit, after an acknowledgment of said request to suspend instruction execution.

Fujita discloses a clock control circuit (See Abstract), wherein a clock switching control circuit (i.e., clock state control circuit 4 of Fig. 1) requests a central processing unit to suspend execution of instructions in response to activation of a selected external device select signal (i.e., starting the processing for changing the clocks; See col. 8, lines 10-21), and wherein said clock switching control circuit (i.e., clock state control circuit) is further capable of switching a first clock signal (See col. 9, lines 25-32) which is provided to an external bus interface control circuit (i.e., frequency-divided clock control device 10, 11 and 12 in Fig. 1), after an acknowledgment of said request to suspend instruction execution (See col. 9, 17-24; i.e., wherein in fact that the clock state control circuit stops the operation once, and enters the sleeping state implies that said capability of controlling to switch a first clock signal after an acknowledgment of a request for suspending of said instruction execution. In other words, the clock state control circuit is waiting for the CPU acknowledgement of a request for stopping the operation during the sleeping state).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said clock state control circuit, as disclosed by Fujita, in said clock switching control circuit, as disclosed by Kume, for the advantage of reducing complication in control over operating clock in said clock switching control circuit (i.e., clock control circuit) and realizing more precise and accurate control over an operating speed (See Fujita, col. 10, lines 57-60).

Referring to claim 7, Fujita teaches said clock switching control circuit (i.e., clock state control circuit 4 of Fig. 1) is capable of switching said first clock signal of said central processing unit in accordance with switching said clock signal of said external bus interface control circuit (i.e., by way of changing clock source of frequency-divided clock control device; See col. 9, lines 33-54).

11. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kume [JP 405341872 A] in view of Yanagiuchi [US 5,684,418 A].

Referring to claim 8, Kume discloses a semiconductor module (i.e., multiprocessor system in Fig. 2) on a module substrate (e.g., PCB in said multiprocessor system) including a plurality of external connection electrodes (i.e., a plurality of connectors for connecting among Data Bus 9, System Address Bus 10, microprocessor 1, the first external data processing device 22, the second external data processing device 23, etc. in Fig. 2) and a plurality of wiring layers (i.e., a plurality of PCB routing layers for the plural signals of Buses, Devices and Clock), said semiconductor module comprising: a microprocessor chip (i.e., microprocessor 1 of Fig. 2) including a clock pulse generator (i.e., clock generator 30 and counting down circuit 19 in Fig. 1) for generating a first clock signal, a second clock signal and a third clock signal (i.e., said counting down circuit generates a plurality of clock signals, such as said first, second and third clock signals in Fig. 1); and a memory chip (i.e., the first external data processing device 22 of Fig. 2) operating synchronously with said first clock signal (i.e., clock signal for the first external data processing device, e.g., fast memory device), wherein said second clock signal (i.e., clock signal for the second external data processing device 23 of Fig. 2, e.g., slow memory device) has a frequency lower than said first clock signal (i.e., the second clock being slower than the first clock signal), wherein said third clock signal has a frequency different from said first clock signal and different from said second clock signal, wherein said clock pulse generator supplies, in parallel, said first and second clock signals external to said microprocessor chip (i.e., said counting-down circuit generates different frequencies on the parallel signal lines, and being provided to external devices in Fig. 1), wherein said microprocessor chip is capable of accessing said memory chip (i.e., the first external data processing device) synchronously with said first clock signal (See col. 5, para. [0025]), and wherein said microprocessor chip is capable of accessing an external device (i.e., an external access through the external data bus 9 and the

external system address bus 10 to the second external data processing device 23 in Fig. 2) synchronously with said second clock signal (See col. 5, para. [0025]).

Kume does not teach clock output pins for supplying in parallel said first and second clock signals to outside.

Yanagiuchi discloses a clock signal generating system (Fig. 1) comprising a clock pulse generator (i.e., clock generator 1 of Fig. 1) and a clock switching control circuit (i.e., clock selector 2 of Fig. 1), wherein clock output pins (i.e., clock signal output lines from said clock generator 1 in Fig. 1) supplying in parallel a first clock signal and a second clock signal generated by said clock pulse generator to outside (See col. 3, lines 26-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said clock generator and said clock selector in said clock signal generating system, as disclosed by Yanagiuchi, for said clock pulse generator and said clock switching control circuit, respectively, as disclosed by Kume, for the advantage of providing a clock signal generator which can make a multiplier and a frequency divider generating a frequency which is not being used stop and thereby prevent needless power consumption and achieve a low power consumption of a system or chip as whole (See Yanagiuchi, col. 1, lines 44-49).

Referring to claim 9, Kume teaches said microprocessor chip (i.e., microprocessor 1 of Fig. 1) comprises: a central processing unit (i.e., CPU 2 of Fig. 1) for executing instructions (See Fig. 1 and col. 5, para. [0022]; i.e., wherein in fact that the Fig. 1 shows the address bus 8 and the data bus 7 coupled to said central processing unit, and said central processing unit outputting access address inherently anticipates that said central processing unit executing instructions) and for operating based on said third clock signal (i.e., said central processing unit accessing said external processing device using said third clock signal, which is generated by said counting down circuit); and an external bus interface control circuit (i.e., micro controller 15, control register 14 and clock selection logic 18 in Fig. 1) for controlling

an external bus (i.e., system data bus 9 and system address bus 10 in Fig. 1) based on execution of instructions by said central processing unit (i.e., a basis of external access operation by said central processing unit; See col. 4, para. [0021]), wherein said central processing unit and said external bus interface control circuit are built in a single chip (See Fig. 1; i.e., said microprocessor 1 implementing CPU 2 and components for external bus interface control in Fig. 1), wherein said external bus interface control circuit is capable of activating a memory chip select signal for selecting said memory chip (i.e., the first external processing device 22 of Fig. 2) in response to an external access address and an external device select signal for selecting an external device (i.e., the second external processing device 23 of Fig. 2) connected to said microprocessor chip through one of said external connection electrodes (i.e., an external access through the external data bus 9 and the external system address bus 10 to the second external data processing device 23 in Fig. 2), i.e., said external bus interface control circuit is capable of activating either a memory chip select signal (i.e., the first external processing device selection) or a second external device select signal (i.e., the second external processing device selection) corresponding to an external access address (See col. 5, para. [0029] and [0030]), wherein said microprocessor chip includes a clock switching control circuit (i.e., clock output selection switch 20 of Fig. 1) capable of: switching a synchronous clock signal of said external bus interface control circuit to a first clock signal in response to activation of said memory chip select signal, and switching said synchronous clock signal of said external bus interface control circuit to a second clock signal in response to activation of said device select signal, i.e., switching said synchronous clock signal to a first clock signal in accordance with activation of said memory chip select signal, and changing to a second clock signal in accordance with activation of said device select signal (See col. 5, para. [0024]).

12. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kume [JP 405341872 A] in view of what was well known in the art, as exemplified by Tymchenko [US 6,026,231 A].

Referring to claim 10, Kume discloses a data-processing system (i.e., multiprocessor system in Fig. 2) comprising: a first signal wire (i.e., clock wire 21 to the first external data processing device 22 in Fig. 2) for transferring a first pulse signal (i.e., clock signal for the first external data processing device, e.g., fast memory device); a second signal wire (i.e., clock wire 21 to the second external data processing device 23 in Fig. 2) for transferring a second pulse signal (i.e., clock signal for the second external data processing device, e.g., slow memory device) with a frequency lower than said first clock signal (e.g., the second clock being slower than the first clock signal); a first device (i.e., the first external data processing device 22 of Fig. 2) operating in accordance with said first pulse signal applying through said first signal wire (See Fig. 2); a second device (i.e., the second external data processing device 23 of Fig. 2) operating in accordance with said second pulse signal (See col. 5, para. [0025]); and a third device (i.e., microprocessor 1 of Fig. 2) capable of controlling accesses to said first device in accordance with said first pulse signal and capable of controlling accesses to said second device in accordance with said second pulse signal (See col. 5, para. [0029] and [0030]), wherein said third device (i.e., microprocessor) wherein said third device (i.e., clock generator 30 and counting-down circuit 19 within said microprocessor 1 in Fig. 1) generates said first pulse signal, said second pulse signal and a third pulse signal (i.e., a plurality of pulse signals are generated by said counting down circuit in Fig. 1).

Kume does not expressly teach said first signal wire, said second signal wire, said first device, said second device and said third device are provided on a mounting board.

The Examiner takes Official Notice that said first clock wire, said second clock wire, said first device, said second device and said third device are provided on a mounting board (e.g., PCB board), is well known to one of ordinary skill in the art of data processing system, as evidenced by Tymchenko (See Fig. 1 and col. 2, lines 63+; i.e., wherein in fact that a plurality of oscillator output wires (i.e., a first clock wire, a second clock wire, etc.), a plurality of CPUs and Memories (i.e., a first device, a second device, and a third device, etc.) are provided on a computer system 10 in Fig. 1(i.e., a mounting board) suggests

said first clock wire, said second clock wire, said first device, said second device and said third device are provided on a mounting board).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented said first clock wire, said second clock wire, said first device, said second device and said third device on a mounting board (e.g., computer system mother board) since it would improve the reliability of said data-processing system.

Referring to claim 11, Kume discloses all the limitations of the claim 11including said mounting board comprising a first circuitry (i.e., microcomputer in Fig. 2) including a first board wire (i.e., Data Bus 9 of Fig. 2) coupled to said second device (i.e., the second external device 23 of Fig. 2); and a second circuitry (i.e., microprocessor 1 of Fig. 2) including a second board wire (i.e., Data Bus 7 of Fig. 1) coupled to said first board wire (i.e., Data Bus 9 of Fig. 1), said first device (i.e., connected to the first external device 22 through said Data Bus 9 in Fig. 2) and a third device (i.e., connected to microprocessor 1 in Fig. 1) except that does not expressly teach said first circuit is implemented on a circuit board, i.e., a first circuit board, and said second circuit is implemented on another circuit board, i.e., a second circuit board.

The Examiner takes Official Notice that said first circuitry being implemented on a first circuit board, and said second circuitry being implemented on a second circuit board, is well known to one of ordinary skill in the art of data processing system, as evidenced by Tymchenko (See Fig. 1 and col. 2, lines 63+; i.e., wherein in fact that a plurality of CPU modules (i.e., a first circuitry and a second circuitry) are implemented on a plurality of CPU boards (i.e., circuit board)).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented each of said first circuitry and said second circuitry on the respective circuit board since it would reduce the repairing/diagnostic service time when said data-processing system is in failure.

Referring to claim 12, Kume teaches said third device is a microprocessor on a single semiconductor chip (i.e., microprocessor 1 of Fig. 1) comprising a central processing unit (i.e., CPU 2 of Fig. 1) for executing instructions (See Fig. 1 and col. 5, para. [0022]; i.e., wherein in fact that the Fig. 1 shows the address bus 8 and the data bus 7 coupled to said central processing unit, and said central processing unit outputting access address inherently anticipates that said central processing unit executing instructions), an external bus interface control circuit (i.e., micro controller 15, control register 14 and clock selection logic 18 in Fig. 1) for controlling an external bus (i.e., system data bus 9 and system address bus 10 in Fig. 1) based on execution of instructions by said central processing unit (i.e., a basis of external access operation by said central processing unit; See col. 4, para. [0021]), wherein said external bus interface control circuit is capable of activating a first external device select signal for selecting said first device or a second external device select signal for selecting said second device in accordance with an external access address, i.e., said external bus interface control circuit is capable of activating either a first external device select signal or a second external device select signal corresponding to an external access address (See col. 5, para. [0029] and [0030]), wherein said third device (i.e., microprocessor of Fig. 1) further includes a switching control circuit (i.e., clock output selection switch 20 of Fig. 1), and wherein said switching control circuit is capable of switching a pulse signal of said external bus interface control circuit to: said first pulse signal in response to activation of said first external device select signal, and said second pulse signal in response to activation of said second external device select signal, i.e., switching said synchronous clock signal to a first pulse signal in accordance with activation of said first external device select signal, and changing to a second pulse signal in accordance with activation of said second external device select signal (See col. 5, para. [0024]).

13. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kume [JP 405341872 A] as applied to claims 10-12 above, and further in view of Yanagiuchi [US 5,684,418 A].

Referring to claim 13, Kume discloses all the limitations of the claim 13 including a pulse signal control circuit (i.e., clock generator 30 and counting down circuit 19 in Fig. 1) and pulse output pin (i.e., pin for clock signal line 21 in Fig. 1), wherein said pulse signal control circuit generates said first pulse signal and said second pulse signal, said first and second pulse signals being different from said third pulse signal (i.e., said counting-down circuit generates different frequencies on the parallel signal lines, such as said first, second and third pulse signals in Fig. 1), and wherein said pulse signal output pin applies said first and second clock signals generated by said pulse signal control circuit in parallel to said first device and second devices, respectively (i.e., one of the clock signals generated in parallel by said counting down circuit is applied to the external devices, respectively) except that does not teach clock output pins apply said first and second clock signals generated by said pulse signal control circuit in parallel to said first device and second devices.

Yanagiuchi discloses a clock signal generating system (Fig. 1), wherein pulse output pins (i.e., clock signal output lines from said clock generator 1 in Fig. 1) apply respectively first pulse signal (e.g., clock output from X_2 11-2 in Fig. 1) and a second pulse signal (i.e., clock output from $X_{1/2}$ 12-2 in Fig. 1) generated by a pulse signal control circuit (i.e., clock generator 1 of Fig. 1) in parallel (See col. 3, lines 26-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said clock generator and said clock selector in said clock signal generating system, as disclosed by Yanagiuchi, for said clock pulse generator and said clock switching control circuit, respectively, as disclosed by Kume, for the advantage of providing a clock signal generator which can make a multiplier and a frequency divider generating a frequency which is not being used stop and thereby prevent needless power consumption and achieve a low power consumption of a system or chip as whole (See Yanagiuchi, col. 1, lines 44-49).

14. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kume [JP 405341872 A] in view of Blomgren [US 5,381,543 A] as applied to claim 4 above, and further in view of Fujita [US 6,529,083 B2].

Referring to claim 14, Kume, as modified by Blomgren, discloses all the limitations of the claim 14 except that does not teach said clock switching control circuit requests said central processing unit to suspend execution of instructions in response to activation of a selected external device select signal, and wherein said clock switching control circuit is further capable of switching said first clock signal and said second clock signal to said external bus interface control circuit after an acknowledgment of said request for suspending of said instruction execution.

Fujita discloses a clock control circuit (See Abstract), wherein a clock switching control circuit (i.e., clock state control circuit 4 of Fig. 1) requests a central processing unit to suspend execution of instructions in response to activation of a selected external device select signal (i.e., starting the processing for changing the clocks; See col. 8, lines 10-21), and wherein said clock switching control circuit (i.e., clock state control circuit) is further capable of switching first and second clock signals (See col. 9, lines 25-32) to an external bus interface control circuit (i.e., frequency-divided clock control device 10, 11 and 12 in Fig. 1) after an acknowledgment of said request to suspend instruction execution (See col. 9, 17-24; i.e., wherein in fact that the clock state control circuit stops the operation once, and enters the sleeping state implies that said capability of controlling to switch a first clock signal after an acknowledgment of a request for suspending of said instruction execution. In other words, the clock state control circuit is waiting for the CPU acknowledgement of a request for stopping the operation during the sleeping state).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said clock state control circuit, as disclosed by Fujita, in said clock switching control circuit, as disclosed by Kume, as modified by Blomgren, for the advantage of reducing complication in control over operating clock in said clock switching control circuit (i.e., clock control

circuit) and realizing more precise and accurate control over an operating speed (See Fujita, col. 10, lines 57-60).

Response to Arguments

15. Applicants' arguments with respect to claims 1, 4, 8 and 10 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Williams [US 5,881,271 A] discloses system and method for clock management.

Nagai [JP 2000194437 A] discloses dual clock system.

Miyazaki et al. [US 6,515,519 B1] disclose semiconductor integrated circuit device.

Keegan [US 4,805,195] discloses selectable timing delay circuit.

17. The Examiner refers to Nagai [JP 2000194437 A] reference as a made of record and not relied upon for the claim rejection in the instant Office Action, and it is referred to the original copy of foreign reference in foreign language (i.e., Japanese). The Examiner attaches a machine translated copy of the reference for the convenience of the Applicants. However, the Examiner cautions the Applicants that the Office is not responsible for any erroneous interpretation resulting from inaccuracies between the original foreign language reference and the machine translation of the reference, as the machine translation may not reflect the original precisely.

18. Applicants' amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH

shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
Art Unit 2112

cel/

Glenn A. Auve
Primary Patent Examiner
Technology Center 2100